claims 1, 3 and 9 under 35 USC §103(a) over Koezuka et al. These grounds of rejection are respectfully traversed for the following reasons.

The present invention is directed to a semiconductor device including a resinous substrate having an uneven surface and a resinous layer provided on the uneven surface of the resinous substrate. The resinous layer, in accordance with the present invention, has a planarized surface and a transistor is provided on the planarized surface of the resinous layer. The transistor comprises a semiconductor layer having a source region, a drain region and a channel formation region provided between the source region and drain region and a gate electrode provided adjacent the channel formation region with a gate insulating film therebetween. The semiconductor layer, in accordance with the present invention, comprises silicon. See, for example, amended claim 1.

In contrast, Tsumura et al. discloses the use of π-conjugated copolymer for a channel of a transistor. Tsumura et al does not disclose, as recited in the amended and new claims, a semiconductor film comprising silicon for a source region, a drain region and a channel formation region. A semiconductor film comprising silicon used for the source region, the drain region and the channel formation region, especially a semiconductor film comprising crystalline silicon, can form a high speed operation transistor.

Further, since the present invention as recited in claims 1, 5, 11 and 12 employs a resinous substrate, the weight of the overall device can be decreased and flexibility can be imparted to the device such that the device can be bent. Also, since a resinous substrate is used, even if an external force is applied, the substrate does not break.

Furthermore, by providing a resinous layer on a resinous substrate, a planarized surface is obtained over an uneven surface of the resinous substrate. Where a semiconductor layer is formed on an uneven surface of a resinous substrate, the unevenness imparts undesirable electrical characteristic effects. To overcome such undesirable effects, the present invention provides a transistor on a planarized surface by providing a resinous layer on an uneven surface of a resinous substrate to prevent the uneven surface of the resinous substrate from undesirably affecting the electric characteristics of the transistor.

Since none of Tsumura et al., Wakai et al. and Koezuka et al. taken alone or in combination discloses or suggests the presently claimed invention, Applicants respectfully request that the §102(e) and §103(a) rejections be reconsidered and withdrawn.

In view of the above, all of the claims in this case are believed to be in condition for allowance. Should the Examiner deem that any further action by the Applicants would be desirable in placing this application in even better condition for issue, the Examiner is requested to contact the undersigned.

Respectfully submitted,

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.

Eric J. Robinson
Registration No. 38,285

EJR/LDE/kmj
Attorney Docket No.: 0756-1838

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
Telephone (703) 790-9110

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